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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,065	09/28/2000	Michael Anthony Perez	AUS9-2000-0452-US1	7603

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EXAMINER
VO, TIM T

ART UNIT	PAPER NUMBER
2189	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/671,065	Applicant(s) PEREZ, MICHAEL ANTHONY	
	Examiner Tim T. Vo	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-28 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 8-14, 20-21 and 27-28 are rejected under 35 U.S.C. § **102(e)** as being anticipated by Anderson et al. patent number 6,338,119 referred hereinafter "Anderson".

As for claims 8, 20 and 27, Anderson teaches a method of providing data to an I/O adapter from a bus bridge (see figure 1, bus bridge 108, I/O devices 118, 120 and column 5 lines 8-11, wherein the bus bridge 108 are transferring data to the I/O devices 118, 120 via a conventional adapter), the method comprising:

receiving a request for data form the I/O adapter (see figure 1, bridge 108 and column 7 lines 8-10 and column 7 lines 45-49, wherein figure 1 discloses I/O devices 118, 120 which are communicating with symmetric multi-processors (SMP) 102 via bridge 108 and conventional adapter and vice versa for the SMP to communicate with

the I/O devices 118, 120. Further, bridge 108 maintains cache 109 coherency as cited in column 4 lines 63-67);

responsive to a determination that the requested data is contained within a cached memory (see figure 1, cache 109), providing the requested data using the data in the cached memory (see figure 1, PCI host bridge 108, cache 109, figure 4 step 406 and 7 lines 6-10, wherein the PCI host bridge determined whether cache 109 is valid or invalid).

As for claims 9, 21 and 28, Anderson teaches responsive to a determination that the requested data is not contained within the cached memory (see figure 1, I/O 118, 120, memory 110 and column 5 lines 1-7, wherein the I/O devices 118, 120 are transferring data to and from system memory 110).

storing the data received from the system memory in the cached memory (see figure 1, system memory containing 130-136 buffers and column 5 lines 22-33, wherein the data are transferred from buffers 130-136 of system memory to cache); and

providing at least a portion of the data received from the system memory to the requesting I/O adapter (see figure 1, I/O 118, 120, system memory 110 and column 5 lines 1-7, wherein I/O devices 118, 120 are transferring data to and from system memory 110).

As for claim 10, Anderson teaches a peripheral component interconnect to peripheral component interconnect bridge (see figure 1, I/O devices 118, 120, conventional adapter and column 5 lines 1-11, wherein I/O devices 118, 120 are connected to conventional adapter i.e. bridge), comprising:

an interface for sending and receiving data from a PCI host bridge (see figure 1, PCI host bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via PCI host bridge 108 and conventional adapter);

an interface for sending and receiving data from an input/output adapter (see figure 1, PCI host bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via PCI host bridge 108 and conventional adapter);

buffers for storing data (see cache 109, system memory 110);

an interface for receiving signals from the PCI host bridge indicating whether data in the buffers are stale (see figure 4, step 406 and column 7 lines 8-22, wherein the PCI host bridge determines whether cache 109 is invalid i.e. stale); and

logic for clearing stale data from the buffers and retrieving fresh data from the PCI host bridge (see column 4 lines 63-67 and column 5 lines 27-33, wherein one of the embodiment, Anderson teaches the PCI host bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

As for claims 11-14, Anderson teaches an interface for receiving signals from the PCI host bridge selecting one of a plurality of modes for handling stale data in the peripheral component interconnect to peripheral component interconnect bridge (see figure 4, step 406 and column 7 lines 8-22, wherein the PCI host bridge determines whether cache 109 is invalid i.e. stale and see column 4 lines 63-67 and column 5 lines

27-33, wherein one of the embodiment, Anderson teaches the PCI host bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 15-19, and 22-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson in view of Anderson et al. patent number 4,868,783 referred hereinafter "Anderson#2".

As for claims 1, 15 and 22, Anderson teaches a method for ensuring that data transferring between a bridge and I/O devices (see figure 1, bridge 108, cache 109, wherein cache 109 is located inside of the bridge and figure 4 step 406 and column 7 lines 8-10 and column 7 lines 45-49, wherein figure 1 discloses I/O devices 118, 120 which are communicating with symmetric multi-processors (SMP) 102 via bridge 108 and vice versa for the SMP to communicate with the I/O devices 118, 120. Further, bridge 108 maintains cache 109 coherency as cited in column 4 lines 63-67), the method comprising:

monitoring signals from a host bridge for an indication of the state of the data within the cached memory (see figure 1, PCI host bridge 108, cache 109, figure 4 step

406 and 7 lines 6-10, wherein the PCI host bridge determined whether cache 109 is valid or invalid); and

responsive to a determination that data in a portion of the cached memory is stale, clearing at least the portion of the cached memory containing the stale data (see column 4 lines 63-67 and column 5 lines 27-33, wherein one of the embodiment, Anderson teaches the PCI host bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

Anderson teaches bus bridge (conventional adapter) to connect I/O devices 118, 120 but Anderson does not expressly teach wherein the conventional adapter contain cache memory. However, Anderson#2 teaches a conventional adapter containing memory (see figure 1, device adapter 25, memory register 31, 45, 42). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Anderson#2 into the teachings Anderson because Anderson#2 providing an improved interconnect system by using configuration register 31 to control communication between a controller and a plurality of associated local or remote terminal devices (see column 1 line 65 to column 2 line 5).

As for claims 2, 16 and 23, Anderson teaches retrieving updated data corresponding to the stale data (see column 5 lines 22-55, wherein cache coherency is updated by 4K page buffer); and storing the updated data in the cached memory (see column 5 lines 28-34, wherein old data in the cache is deleted to make room for new data to be stored).

As for claims 3, 17 and 24, Anderson teaches wherein the signals are sideband signals (see figure 1 buses 112, 116, wherein each buses comprises side band signals).

As for claims 4-5, 18-19 and 25-26, Anderson teaches wherein the signals indicate which pages within the cached memory are stale, and only those pages within the cached memory that are state are discarded (see column 5 lines 22-55, wherein the cache coherency is updated by 4K page buffer and stale data are deleted to make room for new data).

As for claim 6, Anderson teaches wherein the bus bridge is a peripheral component interconnect to peripheral component interconnect bridge (see column 5 lines 8-11, wherein conventional adapter is a bus bridge).

As for claim 7, Anderson teaches wherein the host bridge is a peripheral component interconnect host bridge (see figure 1, PCI host bridge 108).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Tim T. Vo
Examiner
Art Unit 2189

T.V
April 4, 2003